ATTORNEY DOCKET NO. : GREYWALL 16

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Dennis S. Greywall
Serial No.:	09/715,575
Filed:	November 18, 2000
For:	ARTICLE COMPRISING A MEMS DEVICE AND METHOD THEREFOR
Group No.:	2882
Examiner:	Chih Cheng G. Kao

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on _____ (Date)
_____ Printed or typed name of person signing the certificate)
_____ (Signature of the person signing the certificate)

Sir:

AFFIDAVIT UNDER 37 C.F.R. §1.131

State of New Jersey §

Dennis S. Greywall, being duly sworn, deposes and states:

1. I am the sole inventor of the claimed subject matter in the Patent Application identified above and an inventor of the subject matter described therein.

2. Prior to February 23, 2000, I conceived of a shutter-type, micro-electro-mechanical systems (MEMS) device and array, as covered by the above-identified Patent Application, as evidenced by the following:

a. Notations of the conception were stated prior to February 23, 2000. These notations are reflected an invention memorandum, which is kept in the regular course of business. A true and correct copy of this invention memorandum is attached hereto as Exhibits A and B. Any dates omitted from Exhibist A and B are prior to February 23, 2000.

b. After the conception of the invention, I evaluated additional theoretical array and design outlays consistent with and covered by the initial disclosure and provided information for subsequent filing of the above referenced Patent Application in the United States Patent and Trademark Office, which was diligently prepared and filed with the USPTO on November 18, 2000.

3. I declare further that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the Application or any patent issuing thereon.

Dennis S. Greywall

Sworn to and subscribed before me this
2nd day of December, 2003.

Notary Public

SUSAN A. SCHUCHARD
NOTARY PUBLIC
STATE OF NEW JERSEY
MY COMMISSION EXPIRES JUNE 5, 2008

EXHIBIT A

Shutter-Type Optical Switches and Attenuators Constructed Using SOI Wafers

Dennis Greywall

Simple shutter-type structures can be used to switch or attenuate optical signals. Miniature versions of these devices that are most compatible with fiber optics can be fabricated using silicon micromachining techniques. Such devices have been made here at Bell Labs using the MUMPS process. In this process, etching one of several thin (2 micron thick) layers of polysilicon deposited onto a silicon substrate creates the shutter plate. The plate is rotated about miniature silicon hinges into a position perpendicular to the substrate and locked into place with latches to become part of a structure that permits either an in plane or an out-of-plane motion. In applications that require light to be reflected from the surface of the plate it is important that the plate remain accurately perpendicular to the substrate and that the plate form a very flat reflecting surface. With hinges and latches and with compressive stress in the polysilicon layers these requirements are difficult to achieve.

These notes describe a micromachined device that does not suffer these drawbacks. It is fabricated using two-sided DRIE processing of a silicon-on-silicon wafer (nearly stress free) and does not require any self assembly. See the figure below. The "mechanical" portion of the device is formed in the top thin layer of the SOI wafer and is attached via the oxide to a thin perpendicular shutter plate etched from the thick "substrate" layer. If a (110) substrate wafer is used, it can be oriented so that the surface of the shutter plate is an atomically flat (111) surface. The size of the plate is limited only by the thickness of the substrate and so can be relatively large (500microns). All shutter plates on a single device (for example in a cross connect type of switch) are accurately parallel to each other since each is a section of the same single crystal. When not actuated the entire structure lies below the surface of the wafer, making it directly compatible with fiber or free space optics. The design also permits control of damping to prevent switch ringing.

The following two pages outline the processing and provide a sample calculation.

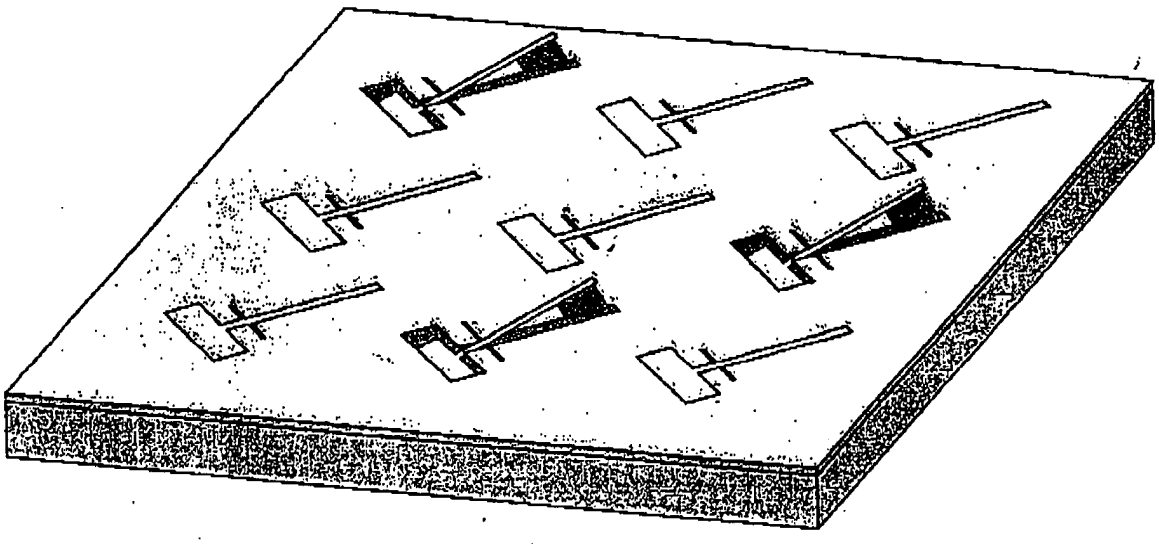

Figure 1.

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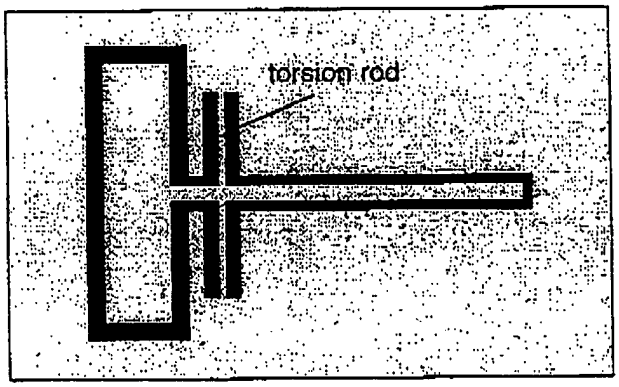
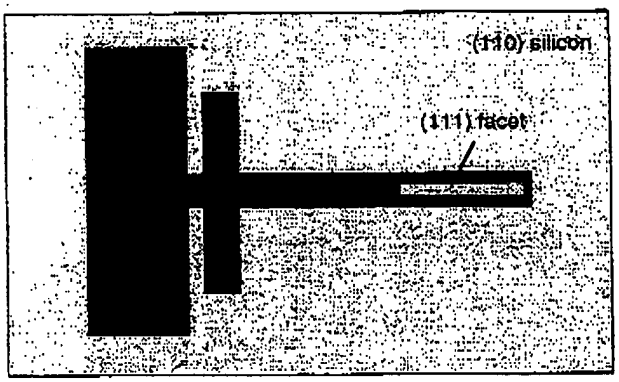
EXHIBIT B

Outline of Process Flow

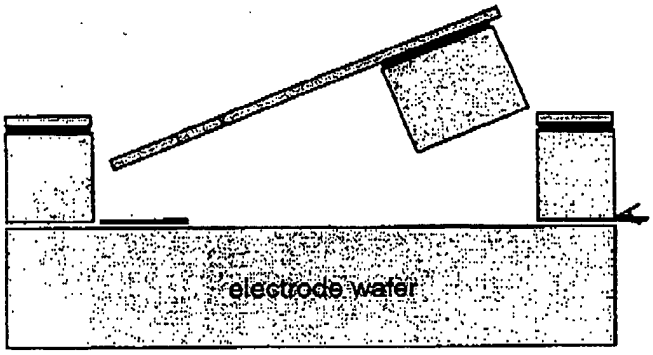


Actuator
Top view of SOI wafer showing pattern RIE etched down to the (black) oxide layer.



Shutter
Bottom view of SOI wafer showing pattern RIE etched down to (black) oxide layer.

After the top and bottom silicon layers are etched, the faces of the shutter plate are washed with a wet etch to clean the (111) facets. The exposed areas of the thin oxide layer are then removed, preferably by dry etching. This leaves the shutter plate attached to the actuator and the actuator free to rotate about the torsional members.



Device
Side view of device showing shutter plate raised by electrostatic force.

wafer bottom

Figure 2.

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Rotation Angle versus Voltage

The devices are made from SOI wafers with a top silicon layer of thickness t and a bottom silicon layer of thickness t_o. Using the other length parameters defined in Figure 3 and assuming that $d/D_1<0.2$, $L=2D_1$ and $w=t$, it can be shown that the voltage and the corresponding rotation angle where snap down occurs are given by

$$V_c \approx 2.6\times10^4 \frac{tt_o^{3/2}}{L_t^{1/2}D_1^2} \quad \text{and} \quad \theta_c \approx 25.2 t_o / D_1 .$$

In these equations lengths are measured in microns and angles in degrees. Figure 4 shows angle versus voltage in reduced units.

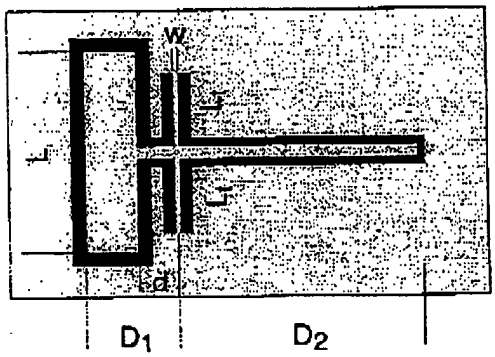

Figure 3

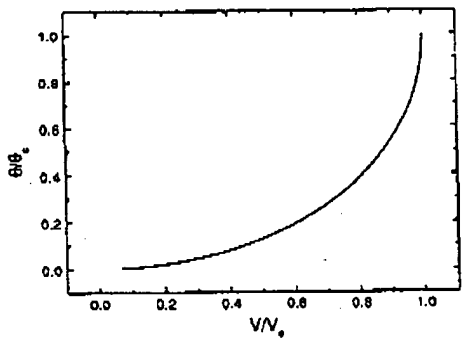

Figure 4

Example:

If $t=2$, $t_o=200$, $D_1=400$, then $V_c = 1810/\sqrt{L_t}$ *and* $\theta_c = 12.6°$. So if $L_t=200$, then $V_c=128volts$. Assuming that the maximum working voltage that would be applied to the device is $0.9V_c=115volts$, the maximum working rotation angle is $0.55\theta_c=7°$.

If $D_2=800$, then the outside edge of the shutter is raised a distance of $800\ tan7° = 100\mu m$ above the surface of the wafer.

example for device performance –

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